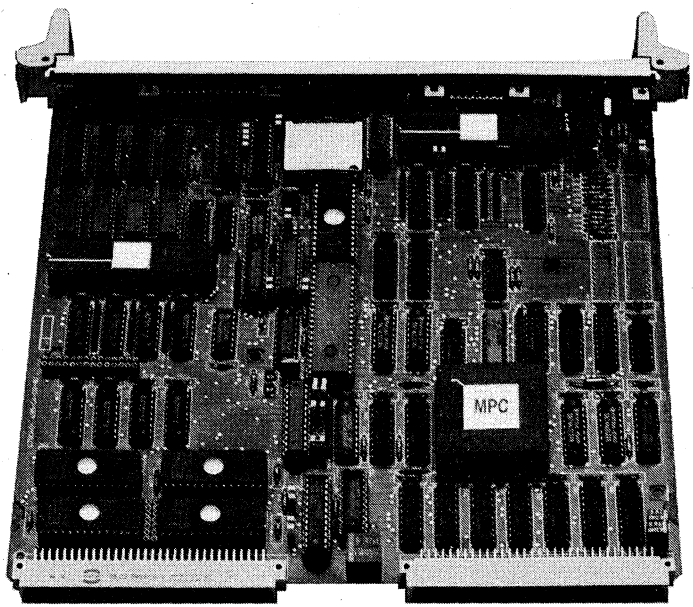
iSBC® 186/530 MULTIBUS® II ETHERNET (IEEE 802.3) COMMUNICATIONS ENGINE

- **Provides ETHERNET (IEEE 802.3) Compatible Networking Capability for all MULTIBUS® II Systems**
- **High Integration 8 MHz 80186 Microprocessor**
- **256K Bytes DRAM Provided, with Sockets to Expand to 512K Bytes DRAM On-Board**
- **MULTIBUS II iPSB (Parallel System Bus) Interface with Full Message Passing Capability**
- **Host Operating System Independent**
- **Four 28-Pin JEDEC Sites, Expandable to 8 Sites with iSBC® 341 MULTIMODULE™ for a Maximum of 512K Bytes EPROM**
- **Provides one RS232C Serial Port for Use in Debug and Testing**
- **MULTIBUS II Interconnect Space for Software Configurability and Diagnostics**
- **Resident Firmware to Support Built-in-Self-Test (BIST) Power-up Diagnostics, and Host-To-Controller Software Download**

The iSBC® 186/530 MULTIBUS® II ETHERNET (IEEE 802.3) Communications Engine is a dedicated ETHERNET communications front-end processor implementing the full, high performance message passing interface of the MULTIBUS II (iPSB) Parallel System Bus. This iSBC board combines an 8 MHz 80186 16-bit microprocessor, an 82586 Local Area Network Coprocessor, an Ethernet Serial Interface component, up to 512K bytes of DRAM, four 28-pin JEDEC sites, and one RS232C serial port on a single 220 mm × 233 mm (8.7 in. × 9.2 in.) Eurocard printed circuit board. Acting as a communications engine, the iSBC 186/530 board off-loads the host CPU(s) in a MULTIBUS II system from managing and executing Ethernet LAN communications tasks. The main advantage of the communications engine concept is the ability to add IEEE 802.3 networking capability to a MULTIBUS II system without requiring a major design effort. The features of the board create a flexible, intelligent communications controller capable of supporting off-the-shelf or custom configurations on IEEE 802.3 LANs.



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Order Number: 280269-002

FUNCTIONAL DESCRIPTION

Overview

The iSBC 186/530 MULTIBUS II ETHERNET Communications Engine is a powerful IEEE 802.3 LAN communications sub-system specifically designed to operate in and support message-based, multiprocessor system configurations being implemented on the MULTIBUS II architecture. The board's on-board CPU, an 8 MHz 80186 microprocessor, provides significant intelligence to off-load and distribute the LAN communications functions away from one or all of a system's processor boards.

The iSBC 186/530 board was designed as a dedicated ETHERNET LAN front-end processor to enable the OEM to connect MULTIBUS II-based systems with different operating systems to the same network.

ARCHITECTURE

The iSBC 186/530 board supports the full iPSB bus interface functions of data and interrupt message passing, interconnect space, memory space, and I/O references. This board supports both requestor and replier functions as described in the MULTIBUS II Architecture Specification Handbook (#146077, Rev. C). The board consists of six major subsystem areas: Processor, ETHERNET I/O, Memory, General I/O, iPSB bus Interface, and Interconnect (See Figure 1).

Processor Subsystem

80186 PROCESSOR

The central processor unit on the iSBC 186/530 board is Intel's 16-bit 8 MHz 80186 microprocessor.

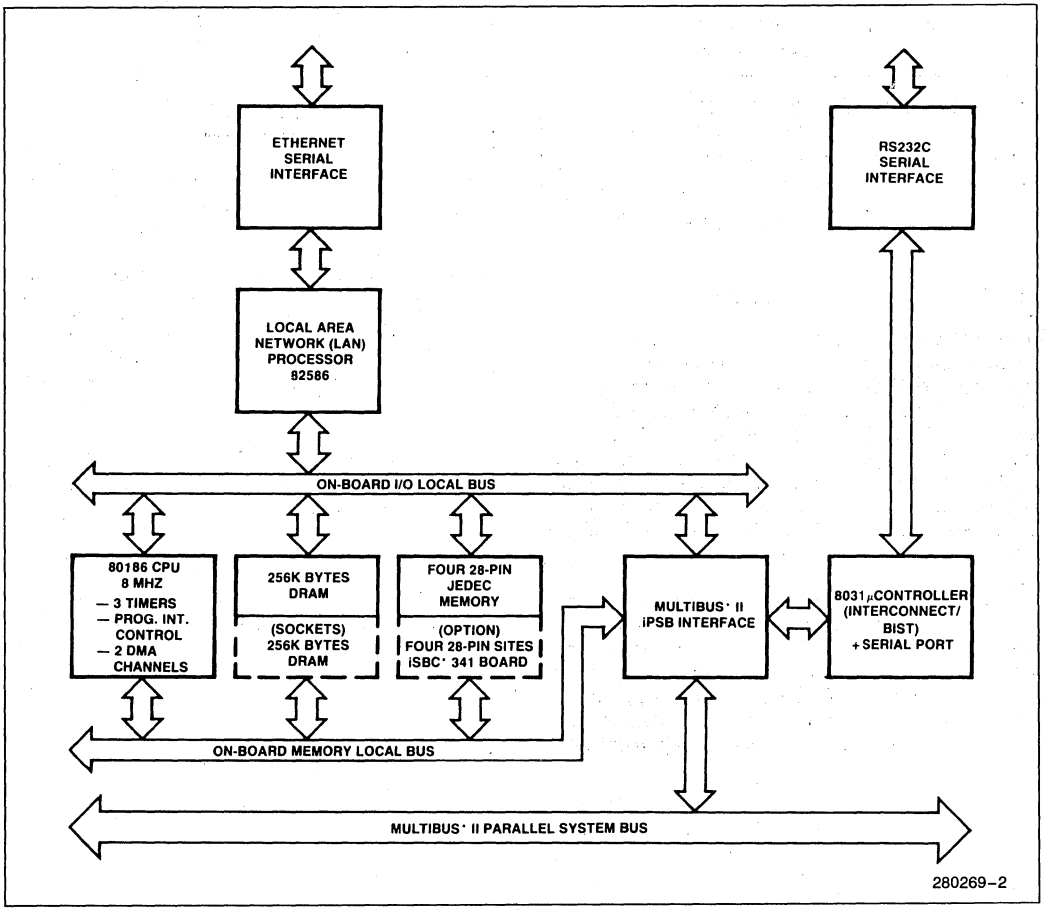

Figure 1. iSBC® 186/530 Board Functional Block Diagram

The highly integrated 80186 CPU combines several system components onto a single chip (i.e., two Direct Memory Access lines, three Interval Timers, Clock Generator, and Programmable Interrupt Controller). The 80186 instruction set is a superset of the 8086 and maintains object code compatibility while adding additional instructions. This high performance component provides the intelligent interface between engine and host processor(s) and manages the board's LAN communications capability. Refer to the Microsystem Components Handbook, Order Number 230843-00X, for more detailed information on the hardware operation and requirements of the 80186 microprocessor component.

DIRECT MEMORY ACCESS (DMA) FUNCTION

The iSBC 186/530 board uses the 80186 microprocessor to provide two DMA channels for DMA support of the iPSB bus interface, the MPC Message Passing Coprocessor chip (See Table 1).

Table 1. iSBC® 186/530 Board DMA Channel Allocation

DMA Configuration (80186)	
80186	**Local Bus Resource**
DMA Channel 0	Output DMA to MPC
DMA Channel 1	Input DMA from MPC (Message Passing Coprocessor)

ETHERNET I/O Subsystem

The ETHERNET interface on the iSBC 186/530 board is implemented by the 82586 LAN Coprocessor and the Ethernet Serial Interface component. Data is transferred between the on-board memory of the iSBC 186/530 board and the 82586 controller by 82586 initiated DMA. The 82586 initiates the DMA cycles by activating the HOLD signal to the 80186 processor. The DMA cycle begins when the 80186 processor activates the HOLD ACKNOWLEDGE signal.

The 82586 component provides most of the functions normally associated with the data link and physical link layers of a local network architecture (See Figure 2). In particular, it performs framing (frame boundary delineation, addressing, and bit error detection), link management, and data modulation. It also supports a network management interface.

The Ethernet Serial Interface component performs Manchester encoding and decoding of the transmit and receive frames. It also provides the electrical interface to the Ethernet transceiver cable. Both chips support a loop-back function. The pin assignments for the Ethernet connector are shown in Table 2.

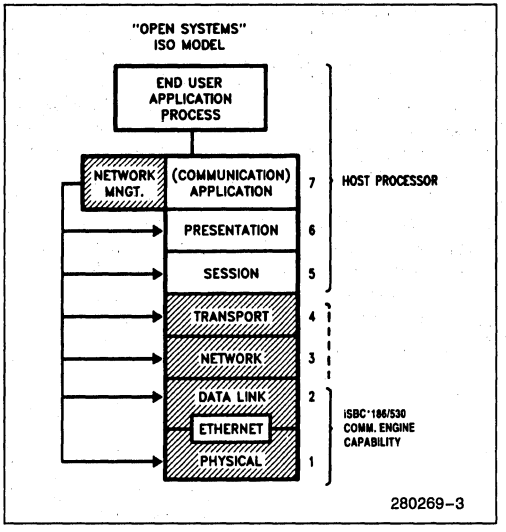

Figure 2. ISO Layered Model and the iSBC® 186/530 Board

Table 2. ETHERNET Connector, Pin Assignments

Pin	Description	Pin	Description
1	Shield	9	Collision (−)
2	Collision (+)	10	Transmit (−)
3	Transmit (+)	11	Reserved
4	Reserved	12	Receive (−)
5	Receive (+)	13	Power
6	Power Return	14	Reserved
7	Reserved	15	Reserved
8	Reserved		

Each iSBC 186/530 board is manufactured with a unique default 48-bit Ethernet network address

stored in an address PROM. This address PROM is protected by checksum and can be read by utilizing the on-board I/O space. The 82586 component can be programmed to have this or any other Ethernet address.

80186/82586 COMMUNICATION

The 80186 and the 82586 communicate entirely through a shared memory space. To the user, the 82586 appears as two independent but communicating units: the Command Unit (CU) and the Receive Unit (RU). The CU executes the commands given by the 80186 to the 82586. The RU handles all activities related to packet reception, address recognition, CRC checking, etc. The two are controlled and monitored by the CPU via a shared memory structure called the System Control Block (SCB). Commands for the CU and RU are placed into the SCB by the host processor. Status information is placed into the SCB by the CU and RU (via the CU). The Channel Attention and Interrupt lines are used by the CPU and the 82586 to get the other to look into the SCB (See Figure 3).

The 82586 features a high level diagnostic or maintenance capability. It automatically gathers statistics on CRC errors, frame alignment errors, overrun errors, and frames lost due to lack of reception resources. In addition, the user can output the status of all internal registers to assist in system design.

Upon initialization, the 82586 obtains the address of its System Control Block through the Initialization Root which begins at location 0FFFFF6H (See Figure 4). The SCB contains control commands, status register, pointers to the Command Block List (CBL) and Receive Frame Area (RFA), and tallies for CRC, Alignment, DMA Overrun, and No Resource errors. Through the SCB, the 82586 is able to provide status and error counts for the 80186, execute "programs" contained in the CBL and receive incoming frames in the Receive Frame Area (RFA).

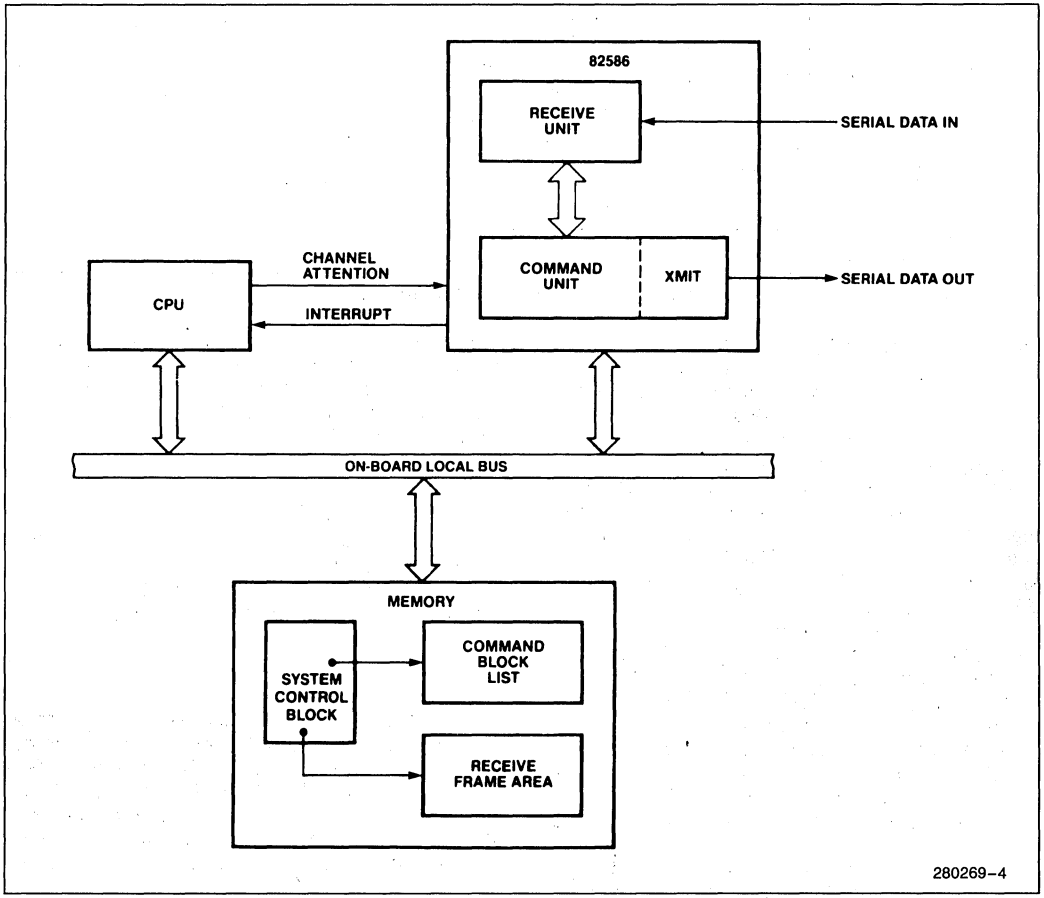

Figure 3. System Overview

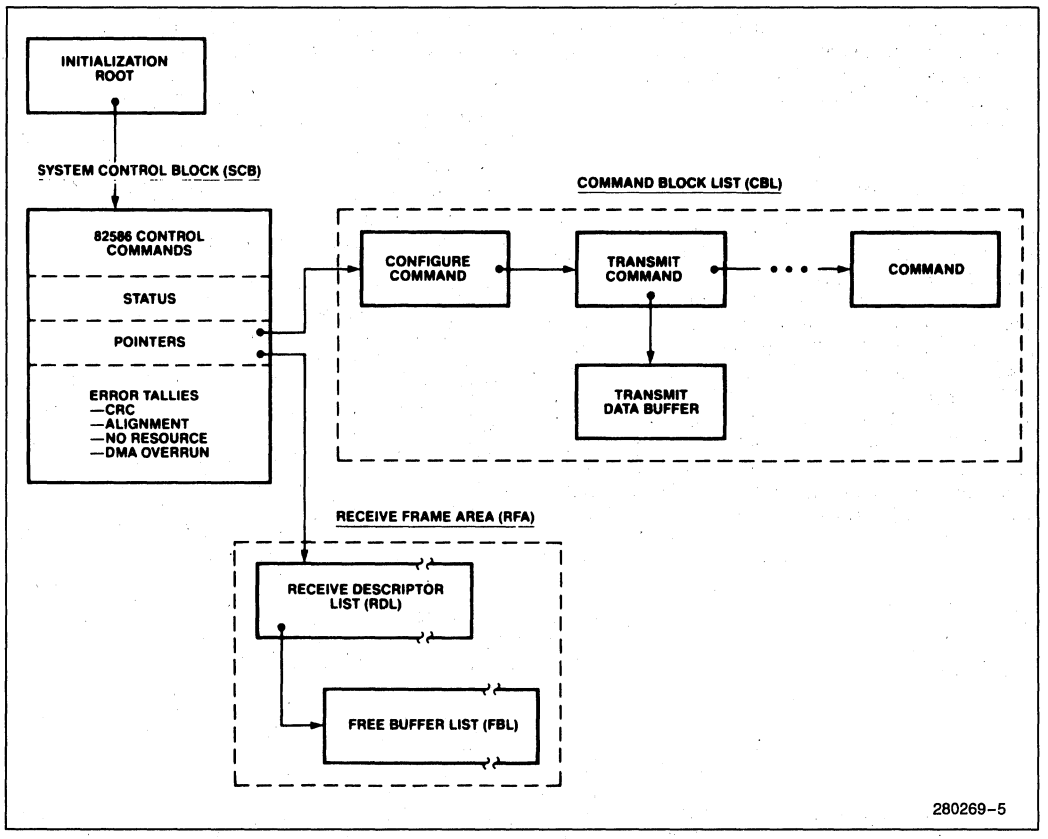

Figure 4. 82586 Memory Structures

Memory Subsystem

The iSBC 186/530 board's on-board memory subsystem consists of a large DRAM array and a set of ROM/EPROM memory sites. Access to the on-board memory subsystem resources, as well as off-board iPSB bus access, is accomplished by observing the iSBC 186/530 board memory map (See Figure 5). The mapping occurs within the 1 megabyte memory space of the 80186 microprocessor, and is split into three main areas: DRAM reserved, iPSB window, and EPROM reserved. The first 0 to 512K bytes is always reserved for local DRAM, the next 128K or 256K bytes (or up to 768K) is the iPSB window, and the remaining 384K or 256K byte area is reserved for local EPROM. The iPSB window maps a 128K or 256K byte memory area into the 4 gigabyte global physical address range of the MULTIBUS II iPSB bus. This window is programmable and allows the 80186 processor to access the complete 4 gigabyte memory space of the iPSB bus.

The board's memory map also supports a 64K byte access window for I/O space between local and iPSB bus access. The 64K bytes of local I/O space is mapped 1-to-1 to the iPSB bus' 64K byte I/O space. The upper 32K bytes access the iPSB bus I/O space, and the lower 32K bytes are reserved for local on-board I/O.

DRAM CAPABILITIES

The iSBC 186/530 board comes standard with a 256K byte DRAM memory array on-board. Eight additional 18-pin sockets are provided to the OEM for expanding the DRAM array to 512K bytes.

EPROM MEMORY

A total of four 28-pin JEDC universal sites reside on the iSBC 186/530 board. These sockets support additon of byte-wide ROM and EPROM devices in densites from 8K bytes (2764) to 64K bytes (27512) per device. Two of the four sockets contain a pair of 27128 EPROM devices installed at the factory. These devices contain 32K bytes of firmware provi-

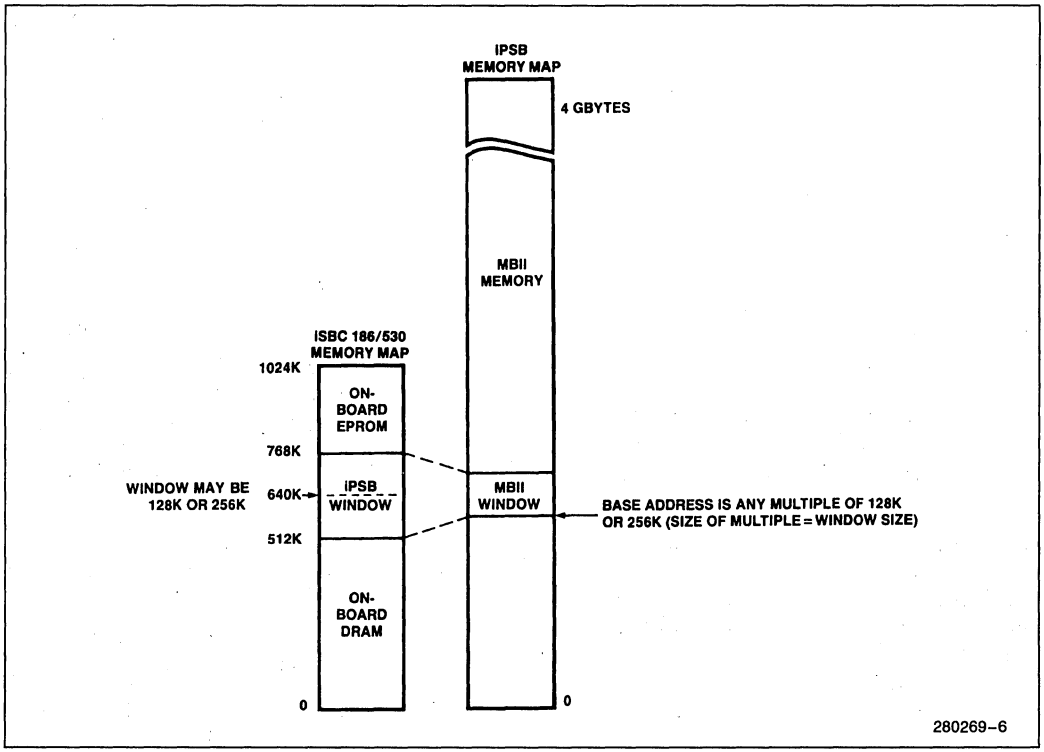

Figure 5. iSBC® 186/530 Board Memory Map Diagram

ded to execute the Built-In-Self-Test (BIST) power-up diagnostics routine, EPROM devices installed at the factory. These devices contain 32K bytes of firmware provided to execute the Built-In-Self-Test (BIST) power-up diagnostics routine. The remaining two sockets allow the user to add either two ROM/EPROM devices or an iSBC 341 256K byte EPROM MULTIMODULE™ board for a maximum of 512K bytes of ROM/EPROM on-board.

General I/O Subsystem

The I/O subsystem provides timers, interrupt control and an RS232C serial port for debug and test.

PROGRAMMABLE TIMERS AND INTERRUPT CONTROL

The board's 80186 microprocessor provides three independent, fully programmable 16-bit interval timers/event counters and an interrupt controller.

The 80186 interrupt controller is configured in the "fully nested mode," and supports five external interrupt sources via five dedicated pins provided on the 80186. All five pins are used as interrupt requests from other hardware on-board (See Table 3).

Table 3. External Interrupt Sources

Interrupt	Vector Type	Vector Location	Default Priority	Function
NMI	2	00008 H	1	Reset stake pin
INT0	12	00030 H	6	Interrupt from the Ethernet Controller
INT1	13	00034 H	7	Message Interrupt from the MPC (MINT)
INT2	14	00048 H	8	Error Interrupt from the MPC (EINT)
INT3	15	0004C H	9	Interrupt from the 8031 Interconnect Controller

RS232C SERIAL PORT

There is a simple RS232C serial port provided on the iSBC 186/530 board for use in debug and test. The serial interface is derived from the 8031 serial interface port. Only the Receive Data (RD) and Transmit Data (TD) lines are supported, connected to a 25-pin connector on the front panel. The pin assignments for the 25-pin connector are shown in Table 4.

Table 4. Serial Interface Connector, Pin Assignments

Pin	RS232CFunction	Pin	RS232C Function
1	Shield	14	Not used
2	Transmit Data (T×D)	15	Not used
3	Receive Data (R×D)	16	Not used
4	Not Used	17	Not Used
5	Not Used	18	Not Used
6	Not Used	19	Not Used
7	Signal Ground (0V)	20	Not Used
8	Not Used	21	Not Used
9	Not Used	22	Not Used
10	Not Used	23	Not Used
11	Not Used	24	Not Used
12	Not Used	25	Not Used
13	Not Used		

iPSB Bus Interface Subsystem

This subsystem's main component is the MPC Message Passing Coprocessor chip. Subsystem services provided by the MPC bus interface component includes full message, memory, I/O, and interconnect access to the iPSB bus by the 80186 and 82586 processors.

The single-chip Message Passing Coprocessor is a highly integrated CMOS device implementing the full message passing protocol and performing all the arbitration, transfer, and exception cycle protocols specified in the MULTIBUS II Architecture Specification Handbook, Rev. C., Order Number 146077.

Interconnect Subsystem

MULTIBUS II interconnect space is a standardized set of read-only and software configurable registers designed to hold and control board configuration information, and communicate system and board level diagnostics and testing information. Interconnect space is implemented with an 8031 microcontroller and the MPC silicon resident on the iSBC 186/530 board.

The read-only registers store information such as, board type, vendor I.D., firmware rev. level, etc. The software configurable registers are used for auto-software configurability and remote/local diagnostics and testing. For example, a software monitor can be used to dynamically change bus memory sizes, enable on-board resources such as memory, read if the PROM devices are installed, or access results of Built-In-Self-Tests and other diagnostics.

Most options on the iSBC 186/530 board are controlled by interconnect space. In addition, many of the interconnect registers on the board perform functions traditionally done by jumper stakes. Other interconnect registers provide status information allowing system software to determine configuration status.

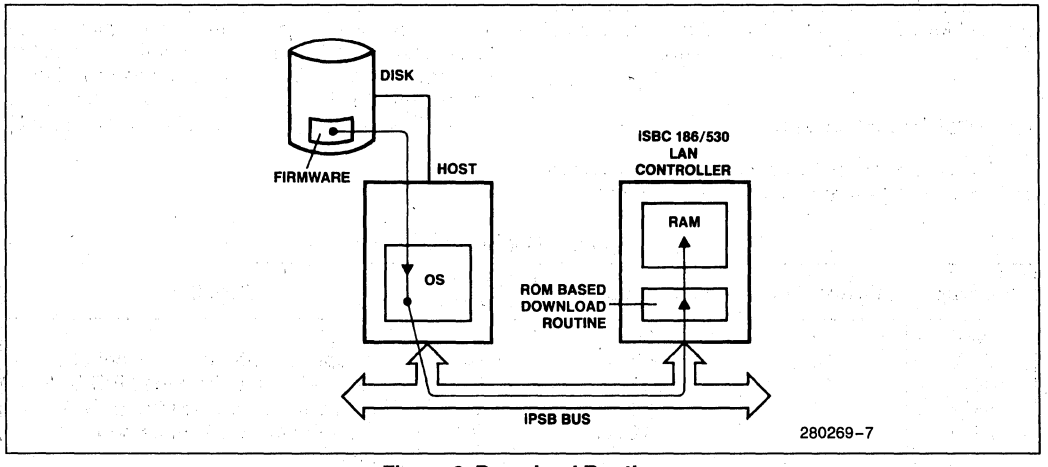

Figure 6. Download Routine

Firmware Capability

HOST/CONTROLLER SOFTWARE DOWNLOAD ROUTINE

Resident in ROM on this controller is a host-to-controller software download routine to support the downloading of communication firmware into the iSBC 186/530 board. This loader adheres to the MULTIBUS II Download Protocol and responds to commands issued by software running on a host CPU board. The host CPU passes these commands to the loader via registers defined in the board's interconnect space. A download function, a commence execution function, and an examine local memory function are all provided in the routine. Data transfers are supported by both shared memory systems and message based systems. The top 1K of DRAM on the board is reserved for the exclusive use of the download program. Host CPUs must not overwrite this area with download commands.

Software on the host is responsible for accessing the iSBC 186/530 board's firmware on disk or from ROM visible to the host and translating it into linear sequences of bytes suitable for downloading (See Figure 6). After downloading the firmware, the host issues a command for the loader routine on the controller to begin execution of the download software.

Built-In-Self-Test Diagnostics

On-board initialization checks and built-in-self-test (BIST) diagnostics are implemented using the 8031 microcontroller and the 80186 microprocessor. On-board tests included in the BIST package are: DRAM, EPROM, 80186, 82586, 8031, and MPC. These tests are performed by the 80186 microprocessor.

Additional activities performed include a Reset Operating System initialization at power-up and a program table check, a feature allowing users to add custom code in EPROM while still maintaining full use of the facory supplied BISTs. Immediately after power-up and the 8031 microprocessor is initialized, the 80186 microprocessor begins its own initialization and on-board diagnostics. Upon successful completion of these activities, the Reset Operation System invokes the user-defined program table. A check is made of the program table and the custom programs that the user has defined for his application will then execute sequentially.

The BIST package provides a valuable testing, error reporting and recovery capability of MULTIBUS II boards enabling OEMs to reduce overall system manufacturing and maintenance costs. An LED on the board's front panel indicates the status of power-up diagnostics. It is on when BIST diagnostics start running and is turned off upon successful completion of the BISTs.

SPECIFICATIONS

Word Size

Instruction—8-, 16-, 24-, or 32-bits
Data—8-, or 16-bits

System Clock

CPU—8.0 MHz

Cycle Time

Basic Instruction—8.0 MHz—375 ns; 250 ns (assumes instruction in queue)

NOTE:
Basic instruction cycle is defined as the fastest instruction time (i.e., two clock cycles).

Memory Capacity

Local Memory

DRAM—256K bytes on-board (64K x 4-bit devices). 8 sockets provided to support additional 256K bytes

EPROM—Number of sockets—four 28-pin JEDEC sites

EPROM	Device Size (Bytes)	Maximum Memory Capacity
2764	8K	32K bytes
27128	16K	64K bytes
27256	32K	128K bytes
27512	64K	256K bytes

**EPROM expansion to up to a maximum of 512K bytes is achieved via attachment of the iSBC 341 EPROM (256K byte) MULTIMODULE board.

I/O Capability

ETHERNET (IEEE 802.3)— One ETHERNET channel. Uses 15-pin connector, 82586 LAN Coprocessor and an Ethernet Serial Interface component

RS232C-only Serial Port— Simple serial port, RS232C, driven off 8031 microcontroller serial port interface; used for debug and test

Timers— Three programmable timers on the 80186 microprocessor

Input Frequencies— Frequencies supplied by the internal 80186 16 MHz crystal

Interrupt Capability

Potential Interrupt Sources from iPSB Bus— 255 individual and 1 Broadcast

Interrupt Levels — 5 interrupt sources using 80186 Interrupt Controller

Interrupt Requests — All levels TTL compatible

Eurocard Form Factor

Depth — 220mm (8.7 inches)

Height — 233mm (9.2 inches)

Front Panel Width — 20mm (0.784 inches)

Weight — 743 g (26 ounces)

Environmental Characteristics

Temperature:	Inlet air at 200 LFM airflow over all boards
(non-operating)	−40°C to +70°C
(operating)	0C° to +55°C
Humidity	
(non-operating)	95% Relative Humidity @ +55°C, non-condensing
(operating)	95% Relative Humidity @ +55°C, non-condensing

Electrical Characteristics

The maximum power required per voltage is shown below. These numbers do not include the power required by the optional memory devices or expansion modules.

Voltage (volts)	Max. Current (amps)	Max. Power (watts)
+5V	6.5A	34.13W
+12V	50 mA	0.06W
−12V	50 mA	0.06W

Reference Manuals

iSBC 186/530 ETHERNET (IEEE 802.3) Communications Engine User's Guide **149226-001**

Intel MULTIBUS II Architecture Specification Handbook **146007**

Reference manuals may be ordered from any Intel Sales Representative, Distribution Office, or from the Intel Literature Department, 3065 Bowers Avenue, Santa Clara, CA 95051.

ORDERING INFORMATION

Part Number	Description
iSBC 186/530	MULTIBUS II ETHERNET (IEEE 802.3) Communication Engine